

REMARKS

At the time of the Office Action dated November 30, 2004, claims 1-4 were pending.

In this Amendment, claims 1-3 have been amended. Care has been exercised to avoid the introduction of new matter. Specifically, claims 1-3 have been amended to require that the second power supply potential is different from the first power supply potential. Adequate descriptive support for this amendment can be found on, for example, page 7, line 4-19 of the specification. Claim 3 has also been amended to replace a "row decoder" with --column decoder-- for correction. In addition, the specification and Fig. 9 have been amended for correction.

Specification.

The Examiner requested correction of errors in the specification. Based on Applicant's review, the specification has been amended, as mentioned above.

Claims 1-4 are pending in this application, all of which have been rejected under 35 U.S.C. §102(b) as being anticipated by Arimoto.

In the statement of the rejection, the Examiner asserted that Arimoto discloses a logic-merged semiconductor memory identically corresponding to what is claimed.

It is well established precedent that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32

USPQ2d 1017 (Fed. Cir. 1994). Applicant submits that Arimoto does not identically disclose a semiconductor memory device including all the limitations recited in claims 1-4 within the meaning of 35 U.S.C. §102.

Arimoto relates to a logic-merged semiconductor memory having a high internal data transfer rate. There are two memory sub arrays in the memory. According to Arimoto, the number of bits of internal data transfer can be increased by carrying out column selection under a state where word lines are selected simultaneously in the two memory sub arrays. See Abstract.

It is submitted that Arimoto does not disclose how two power supply potentials are used. In contrast, the claimed invention provides that, for circuitry around a sense amplifier operated at least two power supply potentials (first and second power supply potentials), the amplitude potentials of the two signals that are input at the time of column operation are the first and second power supply potentials, respectively.

Moreover, the Office Action does not point out where Arimoto discloses relationships between elements and power supply potentials. For example, claims 1-3 recite that a sense amplifier amplifies “a potential difference generated between corresponding bit lines to a potential difference between said first power supply potential and said reference potential.” Claims 1 and 2 recite that a read column decoder turns “the selected read column select line to said second power supply potential at a reading operation” and write column decoder turns “the selected write column select line to said first power supply potential at a writing operation.” Moreover, claim 3 recites that a row decoder turns “the selected first and second column select lines to said first and second power supply potentials, respectively.” The Examiner’s reasoning regarding the rejection and Arimoto is silent with respect to the above described relationship between the claimed elements and power supply potentials.

It is also submitted that Arimoto's transistors T1 to T4 do not correspond to fifth to eighth transistors, recited in claim 1. The Examiner asserted that transistors T1, T2 of Arimoto are "connected in series between a corresponding first bit line and a line of said reference potential" (see the last paragraph on page 5 of the Office Action). According to the Examiner's interpretation of an RGT (see the second paragraph on page 5 of the Office Action), the reference potential in Arimoto's Fig. 18 may be considered to be ground. If so, transistors T1, T2 are not connected in series between the corresponding first bit line and the line of the reference potential, but between the corresponding first bit line and one of write data lines GIOW.

The Examiner further asserted that a gate electrode of one of transistors T1, T2 is "connected to said first write data line." However, Applicant has found no transistor in Arimoto that is connected to the claimed "first write data line" because the gate of transistor T1 is connected to write column select signal CSLW and the gate of transistor T2 is connected to a write data mask designation signal WM. Write column select signal CSLW and write data mask designation signal WM of Arimoto are not identical to the claimed "first write data line."

Therefore, Arimoto's transistors T1, T2 do not correspond to the claimed fifth and sixth transistors. For the same reasons, Arimoto's transistors T3, T4 do not correspond to the claimed seventh and eighth transistors.

With respect to claim 3, the Examiner did not point out where Arimoto discloses a "column select gate" including first to fourth transistors having connections in a manner recited in claim 3. No discussion regarding claim 3 was made in the Office Action.

Accordingly, Applicant submits that Arimoto does not identically disclose a semiconductor memory device including all the limitations recited in independent claims 1-3.

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Dependent claim 4 is patentably distinguishable at least because it includes all the limitations of independent claim 3. Therefore, Applicant respectfully solicits withdrawal of the rejections of claims 1-4 under 35 U.S.C. §102 and favorable consideration thereof.

Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

A handwritten signature in black ink, appearing to read "Tomoki Tanida", written over a horizontal line.

Tomoki Tanida
Recognition under 37 C.F.R. 10.9(b)

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Amendments to the Drawings

The attached sheet of drawings includes changes to Fig. 9. This sheet replaces the original sheet including Fig. 9. In Fig. 9, a write data line “DLW” is replaced with --/DLW--, and a write data line “/DLW” is replaced with --DLW--.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

FIG.9

